APPENDIX A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (Amended) A packaged semiconductor device consisting essentially of [comprising]:

a semiconductor die;

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer, and

at least one void formed in said laminate so as to extend from said first major face through said electrically conductive layer, through said underlying substrate and through said second major face; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major surface of said laminate, wherein said encapsulant is further positioned to extend through said void from said first major face to said second major face and contacting said underlying substrate.

7. (Amended) A packaged semiconductor device consisting essentially of[comprising]:

a semiconductor die;

a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and

at least one void formed in said laminate so as to extend from said first major face through said solder resist layer, through said electrically conductive layer, through said underlying substrate and through said second major face; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

8. (Amended) A packaged semiconductor device consisting essentially of [comprising]:

a semiconductor die;

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

13. (Amended) A packaged semiconductor device consisting essentially of[comprising]:

a semiconductor die;

an epoxy resin glass-cloth laminate defining first and second major faces and including a plurality of laminated epoxy layers, said epoxy laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated epoxy layers; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major face of said epoxy resin glass-cloth laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated epoxy layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

23. (Amended) A computer including at least one packaged semiconductor device consisting essential of[comprising]:

a semiconductor die;

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer,

at least one void formed in said laminate so as to extend from said first major face through said electrically conductive layer, through said underlying substrate, and through said second major face; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

32. (Amended) A packaged semiconductor device consisting essentially of[comprising]:

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers;

a semiconductor chip positioned adjacent one of said major faces of said laminate; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

33. (Amended) An encapsulated integrated circuit consisting essentially of[comprising]:

a printed circuit board comprises a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and

at least one void formed in said printed circuit board so as to extend from one of said major faces through said solder resist layer and said electrically conductive layer at least as far as said underlying substrate;

a semiconductor die positioned adjacent one of said major faces of said printed circuit board and being electrically conductive with said printed circuit board; and

an encapsulant positioned to mechanically couple both said encapsulant and said semiconductor die to said printed circuit board, wherein said encapsulant is further positioned to extend into said void.

34. (Amended) An encapsulated integrated circuit consisting essentially of[comprising]:

a printed circuit board comprises a laminate defining first and second major faces, said laminate including a solder resist layer, a resin laminate having at least one selected layer and at least one adjacent laminated layer, and an electrically conductive layer interposed between said solder resist layer and said resin laminate, said laminate includes at least one void formed therein so as to extend from one of said major faces through said solder resist layer and said electrically conductive layer at least as far as said adjacent laminated layer;

a semiconductor die positioned adjacent one of said major faces of said printed circuit board and being electrically conductive with said printed circuit board; and

an encapsulant positioned to substantially cover and mechanically couple both said encapsulant and said semiconductor die to said printed circuit board, wherein said encapsulant is further positioned to extend into said void so as to form an adhesive bond with at least said resin laminate.